NOV U 8 2006

Docket No.: 1592-0155PUS1

<u>REMARKS</u>

Applicants thank the Examiner for the very thorough consideration given the present in this application. Claims 10-27 are now present in this application. No new matter has been added.

In view of the following remarks, Applicants respectfully request that the Examiner withdraw all outstanding rejections and allow the currently pending claims.

Issues Under 35 U.S.C. § 102(b)

Claims 10-27 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Oida et al. (U.S. 5,647,917) (hereinafter Oida '917). This rejection is respectfully traversed.

The present invention is directed to an epitaxial growth method, which comprises, *inter alia*, polishing a substrate so that an angle of gradient is 0.00° to 0.03° or 0.04° to 0.10° with respect to (100) direction in an entire effective area of the substrate, and forming the compound semiconductor layer to have a thickness of 0.5µm or more on the substrate by using the substrate for growth.

Applicants have discovered that the occurrence of aberrant surface morphology can be prevented by using a substrate not having certain plane orientation in the entire area of the substrate when a III-V group compound semiconductor layer is grown to be 0.5μm or more by epitaxial growth on a substrate for growth. Applicants have further discovered that the aberrant surface morphology occurs when the layer is grown to a thickness of 0.5 μm or more on the substrate, but does **not** occur when the layer is grown less than 0.5 μm. Furthermore, Applicants have also discovered that, by polishing the substrate so that an angle of gradient is 0.00° to 0.03° or 0.04° to 0.10° with respect to (100) direction in an entire effective area of the substrate, the

aberrant surface morphology can be prevented even when the compound semiconductor layer is grown to a thickness greater than or equal to 0.5 µm. Because the aberrant surface morphology occurs in the case that the angle of gradient with respect to (100) surface is 0.03° to 0.04°, the substrate of the present invention **does not** (emphasis added) include a portion having such plane orientation.

Oida '917 does not explicitly or implicitly disclose that the compound semiconductor layer is formed to a thickness of 0.5µm or more. Oida '917 is not concerned with the problem of aberrant surface morphology which occurs when the compound semiconductor layer is formed to be 0.5 µm thick or more. Furthermore, Oida '917 fails to disclose or suggest the use of a substrate not having a certain plane orientation in the entire area of the substrate, specifically, between 0.03° and 0.04°, which is excluded from the present claims. Applicants note that the Examiner has not relied upon the text in the disclosure of Oida '917, but rather has made an "inherency" rejection. The Examiner appears to take the position that Figure 2, which is completely silent about layer thickness, discloses a layer that is **necessarily** (emphasis added) 0.5µm or more. Furthermore, the Examiner does not address the limitation regarding the use of a substrate not having a certain plane orientation.

For anticipation under 35 U.S.C. §102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must

Docket No.: 1592-0155PUS1

make clear that the missing descriptive matter is **necessarily present** (emphasis added) in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " *In re Robertson*, 169 F.3d 743, 745, 49 USPO2d 1949, 1950-51 (Fed. Cir. 1999).

Applicants respectfully submit that Oida '917 is completely silent about the thickness of the compound semiconductor layer. Figure 2 of Oida '917 does not cure this deficiency. Furthermore, the Examiner has not presented any evidence to show that the compound semiconductor layer of Figure 2 **necessarily** (emphasis added) has a thickness of 0.5µm or more. As discussed above, even assuming *arguendo* that a thickness of 0.5µm was a possibility (a point which Applicants do not concede) a mere possibility is not sufficient to establish inherency and/or anticipation.

Furthermore, Applicants respectfully submit that Oida '917 is not at all concerned with the problem of aberrant surface morphology and explicitly teaches away from using a substrate that does not have a plane orientation of 0.03° to 0.04° (see column 6, line 56).

Clearly, Oida '917 does not explicitly or implicitly teach each and every limitation of the instant invention and thus fails to anticipate the same. Reconsideration and withdrawal of this rejection are respectfully requested.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all

Docket No.: 1592-0155PUS1

presently outstanding rejections and objections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action and, as such, the present application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Marc S. Weiner, Reg. No. 32,181 at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.14; particularly, extension of time fees.

Dated:

NOV 8 2006

Respectfully submitted,

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5